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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,709	12/20/2001	Benjamim Tang	35706.5800/66	3875

7590 11/24/2006

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EXAMINER	
TSE, YOUNG TOI	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 11/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/029,709	TANG ET AL.	
	Examiner	Art Unit	
	YOUNG T. TSE	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,6,10-14 and 17-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,10-14 and 17-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because the reference characters "TX" and "RX" labeled in the "frequency compensation and sereds" of the second subsystem 2 should be "RX" and "TX", respectively. Further, the word "serdes" labeled on both subsystems 1 and 2 is not understood. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: paragraph [0013], "FIFO" is undefined; paragraph [0042], line 1, "a exemplary" should be "an exemplary"; paragraph [0051], line 12, "804" should be "806"; and paragraph [0055], line 12, "718" should be "1112". Appropriate correction is required.

Claim Objections

3. Claims 1-3, 5-6, 10-14 and 17-29 are objected to because of the following informalities:

In claim 1, lines 1-2, "FIFO (fill-in fill-out) fill level indicator system, said system" should be "fill-in fill-out (FIFO) fill level indicator, said indicator" because a level indicator is shown in figure 9 as the present invention. Also see claims 5, 10 and 11.

In claim 1, line 7, "FIFO registers" should be "first-in first-out (FIFO) registers". Also see claims 5, 10 and 11.

In line 1 of claims 2-3, 6 and 12, "indicator system" should be "indicator".

In claim 13, line 1, "FIFO" should be "fill-in fill-out (FIFO)"; lines 3-4, 5-6 and 9-10, "write state" and "read state" should be "write counter state" and "read counter state", respectively; and line 7, "FIFO" should be "first-in first-out (FIFO)". Also see claims 17 and 18.

In claim 14, lines 1-2, "said state receiving steps comprise receiving asynchronously said states" should be "said write and read clocks are asynchronous".

In claim 19, line 2, "three" should be "three phases".

In claim 20, line 1, "A PLL/DLL dual loop data serializer" should be "A dual loop serializer"; line 9, "FIFO" should be "first-in first-out (FIFO)"; line 10, "having a" should be "including a phase detector, a digital loop filter and said PLL, said"; and line 21, "a PIPO serializer receiving an input from said FIFO" should be "a parallel-in serial-out (PIPO) serializer receiving an input from said FIFO fill level indicator".

In claim 23, line 2, "a difference" should be "a phase difference".

In claim 28, lines 1 and 2, "said PLL" and "said DLL" should be "said" and "said digital", respectively.

In claim 29, line 1, "the data" should be "the dual loop".

Claims 21-22 and 24-27 depend upon claim 20.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 20-29 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The claimed structures of claim 20 do not correspond to the disclosure of the drawings. For example, claim 20 is directly related to the dual loop serializer shown in figure 5. However, as shown in figure 5, the FIFO register (for example, 904 shown in figure 9) is part of the FIFO fill level indicator 522 and the FIFO fill level indicator 522 is not part of the DLL 504. Wherein claims 21-29 depend upon claim 20.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 3, 6, 13-14 and 17-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 3, line 2, is the phrase "a difference" the same as "a phase difference" recited in claim 1, line 12? If they are the same, the claimed subject matter of claim 3 is already covered in claim 1.

In claim 6 (line 2) and claim 13 (line 12), it is unclear what is meant by "a data clock"?

In both claim 17 and claim 18, the determining step, in a comparison module, determines a phase difference. However, none of the further steps of the determining step performs the result of the phase difference.

Claim 19 depends upon claim 18.

In claim 20, line 12, the phrase "a FIFO fill level indicator in said DLL and receiving an input signal from said FIFO register" is not understood.

Claims 21-29 depend upon claim 20.

Allowable Subject Matter

8. The indicated allowability of claims 1-3, 5-6, 10-14 and 17-20 is withdrawn in view of the newly discovered reference(s) to McEachern et al. and Niegel. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-3, 5-6, 10, 13-14 and 17-18 are rejected under 35 U.S.C. 102(b) as being anticipated by McEachern et al. U.S. Patent No. 4,811,340 (hereinafter "McEAchern").

McEachern discloses a synchronization arrangement in figure 1 for synchronizing an asynchronous data into a synchronous data.

Referring to figure 1, the synchronizing arrangement is illustrated for converting an asynchronous serial digital bit stream, referred to as tributary data and incoming on a line 10, into a locally synchronized serial digital bit stream, referred to as synchronized data, on a line 12. Synchronization is effected using positive and/or negative stuffing in a multiplexer 14 under the control of stuff control signals supplied to the multiplexer 14 by a timing and control circuit 16.

The tributary data bits are written into a cyclic store 18, generally referred to as an elastic store, at an address supplied by a write address generator 20 supplied with a recovered clock signal produced by a clock recovery circuit 22 from the tributary data bit stream, and are read from the store 18 to the multiplexer 14 under the control of a read address generator 24 supplied with a local clock signal from the circuit 16. In order to determine when positive or negative stuffing is necessary to establish or maintain synchronization of the data on the line 12, the relative phases of the write and read addresses produced by the generators 20 and 24 are compared in phase comparators 26 and 28 to produce, when necessary, a positive or negative stuff request signal respectively. The stuff request signals are supplied to the circuit 16 which controls the multiplexer 14 to effect the desired stuffing at the next stuffing opportunity, the clock signal supplied by the circuit 16 to the read address generator 24 being gapped accordingly.

More particularly, the elastic store 18 may be an 8-bit store, with the write and read addresses cyclically addressing these 8 locations with an offset of 4 bits between the write and read addresses corresponding to a zero stuffing situation. If the asynchronous incoming tributary data has a slightly lower frequency than the synchronized data, then this offset will increase by one or more bits with the result that the phase comparator 26 produces a positive stuff request, in response to which a positive stuff reduces the offset between the write and read addresses by one bit. Conversely, if the asynchronous tributary data frequency is lower than that of the synchronized data, the offset decreases by one or more bits and the phase comparator

28 produces a negative stuff request which when satisfied increases the offset by one bit.

With respect to claims 1, 3 and 13, the phase comparators or detectors 26 and 28 and the timing and control circuit 16 correspond to the comparison module to determine a phase difference by the phase comparators between the write and read counter states from the write and read generators 20 and 24 to generate positive and negative stuff requests of a fill level, which comprises a number of read counter cycles by the loops (16, 24, 26 and 28). The phase shift is generated from the phase comparators.

With respect to claims 2 and 14, the write clock and the read clock are asynchronous because the input data 10 is asynchronous data and the output data 12 is synchronous data. See column 4, lines 3-11.

With respect to claims 5-6, the elastic store 18 comprises a plurality of digital words (8-bits) corresponding to a frequency offset, wherein the frequency offset is used to generate a phase shift. See column 4, lines 31-46.

With respect to claims 10 and 17, the comparison module corresponds to an alternative embodiment of figure 6 wherein the phase comparator corresponds to the reset counter is clocked by the read clock generated by the timing and control circuit 16 and the phase comparator corresponds to the register is clocked by the read counter state by the read generator.

With respect to claim 18, the phase comparators 26 and 28 receive multiple phases of the write generator 20 and sample the multiple phases with a read counter state from the read generator 24.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

13. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over McEachern et al. in view of Niegel U. S. Patent No. 5,802,122.

With respect to claim 11, as discussed earlier in section 12 above, McEachern disclosed all the claimed subject matter, except, the synchronization arrangement comprises a plurality of phase detectors, but fails to comprise a binary decoder.

Niegel also discloses a related synchronization circuit in figure 2 comprising similar elements, such as, a buffer memory 5, a write generator 6, a read generator 7, a phase detector 8, and a multiplexer 12. In addition to McEachern's synchronization arrangement, Niegel further comprises a coder 10 which can be an encoder or a decoder for decoding the quantized phase signal generated by the phase detector 8.

Therefore, it would have been obvious to on of ordinary skill in the art to include a decoder in McEachern's synchronization arrangement in order to decode the phase detection signal generated by a phase detector as taught by Niegel, for example, to further correct the phase detection signal prior the signal selection by the multiplexer 14.

With respect to claim 12, the phase comparators 26 and 28 receive multiple phases of the write generator 20 and sample the multiple phases with a read counter state from the read generator 24.

14. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over McEachern.

With respect to claim 19 as applied to claim 18 set forth discussed in section 12 above. Although McEachern does not show three phase detectors for generating three phases, McEachern discloses the synchronization arrangement comprising two phase detector for generating two phases. It would have been obvious to one of ordinary skill in the art that if it is capable of providing two phase detectors for generating two phases is also capable of providing three phase detectors for generating three phases in order to detect more clock signals, which depends upon the requirement of a synchronization circuit.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

References Murakami, Urbansky, Mazzurco et al., Eastty et al., Rude, Bleisteiner et al., and Subrahmanyan et al. all are related to synchronization circuits comprising elestic memories, write counters, read counters and logic circuits for comparing the phase difference of the write and read counter states.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOUNG T. TSE whose telephone number is (571) 272-3051. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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